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CLAIMS 1 – 39 (CANCELLED)

40. (Original) An array substrate for X-ray detector, comprising:

a substrate having a switching region and a pixel region;

a gate line on a substrate, the gate line having a gate linking line and a gate pad at the end thereof;

a gate insulation layer on said gate line;

a data line on said gate insulation layer, the data line perpendicularly crossing said gate line to define the pixel region and having a data linking line and a data pad at the end thereof;

a thin film transistor in the switching region near the crossing of the said gate and data lines, the thin film transistor including a gate electrode, an active layer, a source electrode, a drain electrode and said gate insulation layer;

a ground line crossing said pixel region parallel with the data line and having a ground linking line and a ground pad at the end thereof;

a first passivation layer formed of a silicon insulator, the first passivation layer covering said thin film transistor and having a first drain contact hole that exposes the drain electrode and a first ground line contact hole that exposes the ground line;

a gate pad electrode formed on the first passivation layer, the gate pad electrode contacting the gate pad through a first gate pad contact hole that penetrates both the gate insulation layer and the first passivation layer;

a data pad electrode formed on the first passivation layer, the data pad electrodes contacting the data pad though a first data pad contact hole that penetrates the first passivation layer;

a ground pad electrode formed on the first passivation layer, the ground pad electrode contacting the ground pad though a first ground pad contact hole that penetrates the first passivation layer;

a second passivation layer formed of an organic material on the first passivation layer, the second passivation layer covering the gate pad electrode, the data pad electrode and the ground pad electrode, and having a second drain contact hole that exposes the drain electrode and a second ground line contact hole that exposes the ground line;

a first capacitor electrode on the second passivation layer, the first capacitor electrode contacting the ground line through said first and second ground line contact holes;

an auxiliary drain electrode on the second passivation layer, the auxiliary drain electrode contacting the drain electrode through said first and second drain contact holes;

a third passivation layer on the second passivation layer, the third passivation layer covering the auxiliary drain electrode and the first capacitor electrode, and having an auxiliary drain contact hole that exposes said auxiliary drain electrode; and

a second capacitor electrode on the third passivation layer, the second capacitor electrode electrically contacting the drain electrode and overlapping the first capacitor electrode thereby forming a storage capacitor with the first capacitor electrode and the third passivation layer;

wherein the second and third passivation layers have a second gate pad contact hole that exposes the gate pad electrode, a second data pad contact hole that exposes the data pad electrode, and a ground pad contact hole that exposes the ground pad electrode.

41. (Original) The array substrate according to claim 40, further comprising an ohmic contact layer on the active layer.

42. (Original) The array substrate according to claim 40, wherein the gate line, the gate electrode, the gate linking line and the gate pad have a double-layered structure that includes a first layer and a second layer.

43. (Original) The array substrate according to claim 42, wherein the first layer includes aluminum (Al).

44. (Original) The array substrate according to claim 42, wherein the second layer is formed of a metallic material selected from chromium (Cr), tungsten (W) and molybdenum (Mo).

45. (Original) The array substrate according to claim 40, wherein the gate pad electrodes, the data pad electrodes and the ground pad electrodes are formed in the same plane using the same material.

46. (Original) The array substrate according to claim 40, wherein the second capacitor electrode extends over the thin film transistor.

47. (Original) The array substrate according to claim 40, wherein the second passivation layer includes benzocyclobutene (BCB).

48. (Original) The array substrate according to claim 40, wherein the second passivation layer includes acryl-based resin.

49. (Original) The array substrate according to claim 40, wherein the first passivation layer is formed at a temperature of about 230 degrees centigrade.

50. (Original) The array substrate according to claim 40, wherein the silicon insulator includes silicon nitride (SiN_X).

51. (Original) The array substrate according to claim 40, wherein the silicon insulator includes silicon oxide (SiO_2).

52. (Original) The array substrate according to claim 40, wherein the second capacitor electrode electrically contacts the drain electrode via the auxiliary drain electrode.

53. (Original) The array substrate according to claim 40, wherein the third passivation layer is formed of an inorganic material at a temperature of about 230 degrees centigrade.

54. (Original) The array substrate according to claim 53, wherein the inorganic material includes silicon nitride (SiN_X).

55. (Original) The array substrate according to claim 53, wherein the inorganic material includes silicon oxide (SiO_2).

56. (Original) A method of fabricating an array substrate for X-ray detector, comprising:

forming a gate line on a substrate that has a switching region and a pixel region, the gate line having a gate linking line and a gate pad at the end thereof;

forming a gate insulation layer on said substrate to cover said gate line;

forming a data line on said gate insulation layer, the data line perpendicularly crossing said gate line to define the pixel region and having a data linking line and a data pad at the end thereof;

forming a thin film transistor in the switching region near the crossing of the said gate and data lines, wherein the thin film transistor includes a gate electrode, an active layer, a source electrode, a drain electrode and said gate insulation layer;

forming a ground line that crosses said pixel region parallel with the data line and having a ground linking line and a ground pad at the end thereof;

forming a first passivation layer formed of a silicon insulator, the first passivation layer covering said thin film transistor and having a first drain contact hole that exposes the drain electrode and a first ground line contact hole that exposes the ground line;

forming a gate pad electrode on the first passivation layer, wherein the gate pad electrode contacts the gate pad through a first gate pad contact hole that penetrates both the gate insulation layer and the first passivation layer;

forming a data pad electrode on the first passivation layer, wherein the data pad electrodes contacts the data pad though a first data pad contact hole that penetrates the first passivation layer;

forming a ground pad electrode on the first passivation layer, wherein the ground pad electrode contacts the ground pad though a first ground pad contact hole that penetrates the first passivation layer;

forming a second passivation layer formed of an organic material on the said first passivation layer, the second passivation layer covering the gate pad electrode, the data pad electrode and the ground pad electrode, and having a second drain contact hole that exposes the drain electrode and a second ground line contact hole that exposes the ground line;

forming a first capacitor electrode on the second passivation layer, the first capacitor electrode contacting the ground line through said first and second ground line contact holes;

forming an auxiliary drain electrode on the second passivation layer, the auxiliary drain electrode contacting the drain electrode through said first and second drain contact holes;

forming a third passivation layer on the second passivation layer, the third passivation layer covering the auxiliary drain electrode and the first capacitor electrode, and having an auxiliary drain contact hole that exposes said auxiliary drain electrode;

forming a second capacitor electrode on the third passivation layer, the second capacitor electrode electrically contacting the drain electrode and overlapping the first capacitor electrode thereby forming a storage capacitor with the first capacitor electrode and the third passivation layer; and

etching portions of the second and third passivation layers to form a second gate pad contact hole that exposes the gate pad electrode, a second data pad contact hole that exposes the data pad electrode and a ground pad contact hole that exposes the ground pad electrode.

57. (Original) The method of fabricating an array substrate according to claim 56, further comprising forming an ohmic contact layer on the active layer.

58. (Original) The method of fabricating an array substrate according to claim 57, further comprising etching a portion of the ohmic contact layer using the source and drain electrodes as masks so as to form an active channel on the active layer.

59. (Original) The method of fabricating an array substrate according to claim 56, wherein the gate line, the gate electrode, the gate linking line and the gate pad have a double-layered structure that includes a first layer and a second layer.

60. (Original) The method of fabricating an array substrate according to claim 59, wherein the first layer includes aluminum (Al).

61. (Original) The method of fabricating array substrate according to claim 59, wherein the second layer includes a metallic material selected from chromium (Cr), tungsten (W) and molybdenum (Mo).

62. (Original) The method of fabricating an array substrate according to claim 56, wherein the gate pad electrode, the data pad electrode and the ground pad electrode are simultaneously formed in the same plane using the same material.

63. (Original) The method of fabricating an array substrate according to claim 56, wherein the second capacitor electrode extends over the thin film transistor.

64. (Original) The method of fabricating an array substrate according to claim 56, wherein the second passivation layer includes benzocyclobutene (BCB).

65. (Original) The method of fabricating an array substrate according to claim 56, wherein the second passivation layer includes acryl-based resin.

66. (Original) The method of fabricating an array substrate according to claim 56, wherein the first passivation layer is formed at a temperature of about 230 degrees centigrade.

67. (Original) The method of fabricating an array substrate according to claim 56, wherein the silicon insulator includes silicon nitride (SiN_X).

68. (Original) The method of fabricating an array substrate according to claim 56, wherein the silicon insulator includes silicon oxide (SiO_2).

69. (Original) The method of fabricating an array substrate according to claim 56, wherein the first and second capacitor electrodes are formed of indium tin oxide (ITO).

70. (Original) The method of fabricating an array substrate according to claim 56, wherein the first and second capacitor electrodes are formed of indium zinc oxide (IZO).

71. (Original) The method of fabricating an array substrate according to claim 56, wherein the second capacitor electrode electrically contacts the drain electrode via the auxiliary drain electrode.

72. (Original) The method of fabricating an array substrate according to claim 56, wherein the third passivation layer is formed of an inorganic material at a temperature of about 230 degrees centigrade.

73. (Original) The method of fabricating an array substrate according to claim 72, wherein the inorganic material includes silicon nitride (SiN_X).

74. (Original) The method of fabricating an array substrate according to claim 72, wherein the inorganic material includes silicon oxide (SiO_2).